REMARKS

Claims 3-12 are pending in the application. By this amendment, claim 3 is being amended to improve its form; a marked up version of the amended claim is attached hereto pursuant to 37 C.F.R. § 1.121(c)(ii). No new matter is involved.

Beginning at the bottom of page 2 of the Office Action, claims 3-12 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 5,436,875 of Shinada et al. in view of U.S. Patent 5,434,997 of Landry et al. Shinada is said to disclose most of the claimed structure, but not how the system suspends operation or the details of the suspension circuit and data being placed in a suspended state by interrupting the power supply or by halting an operation clock. Landry is said to disclose a data processing circuit for recording data being placed in a suspended state by interrupting the power supply or by halting the supply of an operation clock. This rejection is respectfully traversed.

In accordance with the invention, the operation of a data processing circuit is placed in a suspended state by interrupting the power supply to the data processing circuit or by halting the supply of a data clock to the data processing circuit. Consequently, power consumption can be reduced. It is not a feature of the present invention to simply interrupt the operation when there is no data.

The cited references do not disclose or suggest such a configuration in accordance with the present invention.

As described at lines 7-13 of col. 5 of Shinada, the method used therein is a thermal magnetic recording method adopted to a rewriteable disk, not to a write-once disk such as is used in accordance with the present invention. Further, a disk in Shinada can be regarded as an MB from the description of the area configuration and the data transfer rate.

The present invention involves a write-once disk in which recorded data cannot be erased. Accordingly, a configuration is achieved in which the recorded data is read out and new data is written successively, starting at the address of the

last recorded data. In Shinada, where rewriting on the disk can be performed, such reference does not show or suggest the configuration of the present invention.

Further in Shinada, data is reproduced from a disk and data is written onto the same disk. Specifically, data is read out from a disk and is output via a buffer. At this time, data output from the buffer is performed at a lower rate than data reading from the disk. Therefore, when recording data from the disk, the amount of data stored in the buffer gradually increases. Then, when the amount of data stored in the buffer reaches a predetermined level, data reading from the buffer is stopped. When writing data is written onto the disk via the buffer, on the other hand, data writing onto the disk is performed at a higher rate than data writing onto the buffer, so that the amount of data stored in the buffer gradually decreases. Then, when the amount of data stored in the buffer is below the predetermined level, data writing onto the disk is stopped.

In Shinada, data reproduction from the disk and data recording onto the disk are alternately performed. Although Shinada describes that data recording is performed intermittently in a manner such that data discontinuity can be avoided, there is no detailed description of how data is recorded after resumption of recording.

Shinada also describes interruption of reproducing when an abnormality such as a track jump is detected. In such case, however, write retry is performed using data stored in the buffer. Thus, it is supposed that in Shinada the recorded data is overwritten to some extent, and that rewriting is started from the section at which recording was performed without problems.

In the present invention, on the other hand, data already stored in the disk is read, and data is additionally written on the disk in synchronism with the read data. In this manner, additional data write is enabled without generating gaps, even on a write-once disk such as a CD-R. Such a configuration is not disclosed or suggested by Shinada.

In the upper portion of page 9 of the Office Action, the Examiner states "To this end Shinada is using buffers exactly as claimed and disclosed by the Applicants." However, inasmuch as Applicant's argument is focused on disk recording and reproduction, such a statement is inappropriate. Moreover, while the Office Action states that additional data write is also performed in Shinada, it appears that Shinada contains no description concerning additional writing as claimed in the present invention, and as described above.

As previously noted, Shinada is capable of data recording during data reproduction, and reading and writing with regard to the disk are alternatively performed. On the other hand, and in accordance with the present invention, in order to record data continuously to data recorded immediately before interruption of recording, the timing for additional data write onto the disk is established. Therefore, data which is already recorded is reproduced. Thus, the present invention completely differs from Shinada, even in terms of the object of reproducing.

Claims 3-12 are submitted to clearly distinguish patentably over the art.

In claim 3, for example, such claim has been amended to define a recording data processing circuit for processing received data sent at a slower data transmission speed than a data processing speed at which to write recording data "onto a non-erasable, write-once disk". The circuit is comprised of a buffer memory, a data processing circuit, a system control circuit and a writing circuit. The system control circuit is said to suspend operation of the data processing circuit until an amount of received data equivalent to a predetermined writing capacity has been stored in a buffer memory, and to release suspension of the operation of the data processing circuit when an amount of received data equivalent to the predetermined writing capacity has been stored in the buffer memory. The data processing circuit for recording data is placed in a suspended state "by interrupting the power supply or by halting the supply of an operation clock". Further, the system control circuit "stores an address successive to an address of received data last recorded onto the

disk, as a recording start address on the disk, and controls the writing circuit so as to write the recording data supplied from the data processing circuit onto the disk at the recording start address". Still further, the system control circuit "synchronizes the recording data to be newly recorded onto the disk, supplied from the data processing circuit to the writing circuit, with recording data recorded on the disk, said data processing circuit being operated in synchronism with a reproduction clock obtained by reproducing the data already recorded on the disk". As described in detail above, the prior art does not show or suggest such a recording data processing circuit in accordance with the invention.

Similar comments apply to independent claim 7 which defines a recording data processing circuit in similar fashion, and to claims 2-6 and 8-12 which depend from and contain all of the limitations of their parent claims.

In conclusion, claims 1-12 are submitted to clearly distinguish patentably over the prior art for the reasons discussed above. Therefore, reconsideration and allowance are respectfully requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles telephone number (213) 337-6846 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,

HOGAN & HARTSON L.L.P.

Date: October 7, 2002

By: _____
John P. Scherlacher
Registration No. 23,009
Attorney for Applicant(s)

Biltmore Tower
500 South Grand Avenue, Suite 1900
Los Angeles, CA 90071
Telephone: (213) 337-6700
Facsimile: (213) 337-6701

Version with markings to show changes made:

IN THE CLAIMS:

Rewrite claim 3 as follows:

3. (Three Times Amended) A recording data processing circuit for processing received data sent at a slower data transmission speed than a data processing speed at which to write recording data onto a non-erasable, write-once disk, comprising:

a buffer memory for temporarily storing the received data;

a data processing circuit for preparing the recording data to record onto the disk, based on the received data read from the buffer memory;

a system control circuit for controlling writing and reading of the received data with respect to the buffer memory, and operation of the data processing circuit, and

a writing circuit for writing the recorded data supplied from the data processing circuit, onto the disk,

wherein

the system control circuit suspends operation of the data processing circuit until an amount of received data equivalent to a predetermined writing capacity has been stored in the buffer memory, and releases suspension of the operation of the data processing circuit when an amount of received data equivalent to the predetermined writing capacity has been stored in the buffer memory, said data processing circuit for recording data being placed in a suspended state by interrupting the power supply or by halting the supply of an operation clock,

wherein

the system control circuit stores an address successive to an address of received data last recorded onto the disk, as a recording start address on the disk, and controls the writing circuit so as to write the recording data supplied from the data processing circuit onto the disk at the recording start address,

and wherein

the system control circuit synchronizes the recording data to be newly recorded onto the disk, supplied from the data processing circuit to the writing circuit, with recording data recorded on the disk, said data processing circuit being operated in synchronism with a reproduction clock obtained by reproducing the data already recorded on the disk.